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09/752,874	12/29/2000	Lily P. Looi	2207/9869	1458

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EXAMINER
PATEL, NIMESH G

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,874	LOOI ET AL.	
	Examiner	Art Unit	
	Nimesh G. Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-26* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 9-12, 16-21 and 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Tavallaei et al.(US Patent 5,987,538), hereinafter referred to as Tavallaei.

3. Regarding claim 1, Tavallaei discloses an interrupt delivery system that has a first pair of scaleable node controllers(Figure 2, Component 14; Component 14 is scaleable since the number of Components 14 can change and the system can still function well; See definition of scalability in the "Whatis.com" reference cited), wherein each node controller supports at least 1 microprocessor(Figure 2, Components 12). Tavallaei further discloses a first scalability port switch(Figure 2, Component 26; Component 26 is scalable since the number of interrupts handled can increase) coupled to each of said scaleable node controllers, wherein said first scalability port switch is to receive an interrupt request, determine an ID, i.e. address, of one of said scaleable node controllers from said interrupt request and transmit said interrupt request to said one of said scaleable node controllers(Column 7, Lines 6-9, 54-56; Column 8, Lines 43-46). Tavallaei shows all of the elements recited in claim 1 and therefore, claim 1 is rejected.

4. Regarding claim 2, Tavallaei discloses an interrupt delivery system, further comprising a peripheral component interconnect device(Figure 1, Component 34). Tavallaei shows all of the elements recited in claim 2 and therefore, claim 2 is rejected.

5. Regarding claim 3, Tavallaei discloses an interrupt delivery system, further comprising a peripheral component interconnect bus coupled between the peripheral component interconnect device and the first scalability port switch, wherein said peripheral component interconnect bus is able to support a plurality of additional peripheral component interconnect device(Column 6, Lines 47-53; Component 26 and 28 are integrated and therefore Component 26 is also connected to the PCI bus 32). Tavallaei shows all of the elements recited in claim 3 and therefore, claim 3 is rejected.

6. Regarding claim 9, Tavallaei discloses a method for delivering an interrupt request in a multi-node computer system, comprising: receiving an interrupt request at a scalability port switch(Figure 2, Component 26; Component 26 is scalable since the number of interrupts handled can increase. See definition of scalability in the "Whatis.com" reference cited); determining an ID, i.e. address of a scaleable node controller(Figure 2, Component 14; Component 14 is scaleable since the number of Components 14 can change and the system can still function well) to receive said interrupt request; and transmitting said interrupt request to said scaleable node controller(Column 7, Lines 6-9, 54-56; Column 8, Lines 43-46). Tavallaei shows all of the elements recited in claim 9 and therefore, claim 9 is rejected.

7. Regarding claim 10, Tavallaei discloses a method for delivering an interrupt request in a multi-node computer system, further comprising determining a processor to receive the interrupt request(Column 7, Lines 6-9). Tavallaei shows all of the elements recited in claim 10 and therefore, claim 10 is rejected.

8. Regarding claim 11, Tavallaei discloses a method for delivering an interrupt request in a multi-node computer system, further comprising comparing a priority of the interrupt request

with a priority of the processor(Column 7, Line 41-44). Tavallaei shows all of the elements recited in claim 11 and therefore, claim 11 is rejected.

9. Regarding claim 12, Tavallaei discloses a method for delivering an interrupt request in a multi-node computer system,, further comprising interrupting the processor(Column 7, Lines 6-9). Tavallaei shows all of the elements recited in claim 12 and therefore, claim 12 is rejected.

10. Regarding claim 16, Tavallaei discloses an interrupt request that is generated by a PCI device(Column 4, Lines 62-63). Tavallaei shows all of the elements recited in claim 16 and therefore, claim 16 is rejected.

11. Regarding claim 17, Tavallaei discloses a method, wherein the interrupt request is generated by a processor(Column 4, Line 50). Tavallaei shows all of the elements recited in claim 17 and therefore, claim 17 is rejected.

12. Regarding claim 18, Tavallaei discloses a set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor for delivering an interrupt request in a multi-node computer system, comprising: receiving an interrupt request at a scalability port switch(Figure 2, Component 26; Component 26 is scalable since the number of interrupts handled can increase. See definition of scalability in the "Whatis.com" reference cited); determining an ID, i.e. address of scaleable node controller(Figure 2, Component 14; Component 14 is scaleable since the number of Components 14 can change and the system can still function well) to receive said interrupt request; and transmitting said interrupt request to said scaleable node controller(Column 7, Lines 6-9, 54-56; Column 8, Lines 43-46). Tavallaei shows all of the elements recited in claim 18 and therefore, claim 18 is rejected.

13. Regarding claim 19, Tavallaei discloses a method for delivering an interrupt request in a multi-node computer system, further comprising determining a processor to receive the interrupt request(Column 7, Lines 6-9). Tavallaei shows all of the elements recited in claim 19 and therefore, claim 19 is rejected.

14. Regarding claim 20, Tavallaei discloses a method for delivering an interrupt request in a multi-node computer system, further comprising comparing a priority of the interrupt request with a priority of the processor(Column 7, Line 41-44). Tavallaei shows all of the elements recited in claim 20 and therefore, claim 20 is rejected.

15. Regarding claim 21, Tavallaei discloses a method for delivering an interrupt request in a multi-node computer system,, further comprising interrupting the processor(Column 7, Lines 6-9). Tavallaei shows all of the elements recited in claim 21 and therefore, claim 21 is rejected.

16. Regarding claim 25, Tavallaei discloses an interrupt request that is generated by a PCI device(Column 4, Lines 62-63). Tavallaei shows all of the elements recited in claim 25 and therefore, claim 25 is rejected.

17. Regarding claim 26, Tavallaei discloses a method, wherein the interrupt request is generated by a processor(Column 4, Line 50). Tavallaei shows all of the elements recited in claim 26 and therefore, claim 26 is rejected.

18. Claims 1-3, 9-12, 14-21, and 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Olarig et al.(US Patent 5,944,809), hereinafter referred to as Olarig.

19. Regarding claim 1, Olarig discloses an interrupt delivery system that has a first pair of scaleable node controllers(Figure 4, Component 107, 306; More components of type 107 and 306 can be used and therefore it is scaleable), wherein each node controller supports at least 1

microprocessor(Figure 4, Components 105, 106). Olarig further discloses a first scalability port switch(Figure 4, Component 312; Column 8, Lines 8-12; Since more components of type 312 can be used, it is scalable) coupled to each of said scaleable node controllers, wherein said first scalability port switch is to receive an interrupt request, determine an address of one of said scaleable node controllers from said interrupt request and transmit said interrupt request to said one of said scaleable node controllers(Column 8, Lines 35-40; Column 9, Lines 57-65; LOPICs are bus agents that inherently have an address. By delivering the interrupt request to the destination LOPIC, an address has to be determined to deliver the interrupt request to the proper LOPIC). Olarig shows all of the elements recited in claim 1 and therefore, claim 1 is rejected.

20. Regarding claim 2, Olarig discloses an interrupt delivery system, further comprising a peripheral component interconnect device(Since Olarig discloses a PCI bus(Figure 4, 113; Column 8, Line 1), it is inherent Olarig's system comprises a PCI device). Olarig shows all of the elements recited in claim 2 and therefore, claim 2 is rejected.

21. Regarding claim 3, Olarig discloses an interrupt delivery system, further comprising a peripheral component interconnect bus(Figure 4, 113) coupled between the peripheral component interconnect device and the first scalability port switch, wherein said peripheral component interconnect bus is able to support a plurality of additional peripheral component interconnect device(Column 8, Lines 16-17; Since there are plurality of I/O devices, and there is a PCI bus, there are plurality of PCI devices). Olarig shows all of the elements recited in claim 3 and therefore, claim 3 is rejected.

22. Regarding claim 9, Olarig discloses a method for delivering an interrupt request in a multi-node computer system, comprising: receiving an interrupt request at a scalability port

switch(Figure 4, Component 312; Column 8, Lines 8-12; Since more components of type 312 can be used, it is scalable); determining an address of a scaleable node controller(Figure 4, Component 107, 306; More components of type 107 and 306 can be used and therefore it is scaleable) to receive said interrupt request; and transmitting said interrupt request to said scaleable node controller(Column 8, Lines 35-40; Column 9, Lines 57-65; LOPICs are bus agents that inherently have an address. By delivering the interrupt request to the destination LOPIC, an address has to be determined to deliver the interrupt request to the proper LOPIC). Olarig shows all of the elements recited in claim 9 and therefore, claim 9 is rejected.

23. Regarding claim 10, Olarig discloses a method of determining a processor to receive an interrupt request(Column 9, Lines 57-65), Olarig shows all of the elements recited in claim 10 and therefore, claim 10 is rejected.

24. Regarding claim 11, Olarig discloses a method of comparing a priority of the processor's task with that of the interrupt request(Column 3, Lines 4-7; Column 10, Lines 8-10). Olarig shows all of the elements recited in claim 11 and therefore, claim 11 is rejected.

25. Regarding claim 12, Olarig discloses a method for interrupting the processor(Column 10, Lines 10-13). Olarig shows all of the elements recited in claim 12 and therefore, claim 12 is rejected.

26. Regarding claim 14, Olarig discloses an interrupt request that is a broadcast interrupt(Column 9, Lines 56-67, and Column 10, Lines 1-7; A distributed delivery mode interrupt is a broadcast interrupt). Olarig shows all of the elements recited in claim 14 and therefore, claim 14 is rejected.

27. Regarding claim 15, Olarig discloses the use of an end of interrupt register to indicate the end of processing of an interrupt(Column 7, Lines 50-55). Olarig shows all of the elements recited in claim 15 and therefore, claim 15 is rejected.

28. Regarding claim 16, Olarig discloses an interrupt request that is generated by a PCI device(Column 8, Line 17; Since Olarig discloses a PCI bus(Figure 4, 113; Column 8, Line 1), it is inherent Olarig's system comprises a PCI device that will generate an interrupt). Olarig shows all of the elements recited in claim 16 and therefore, claim 16 is rejected.

29. Regarding claim 17, Olarig discloses a method, wherein the interrupt request is generated by a processor(Column 7, Lines 28-30). Olarig shows all of the elements recited in claim 17 and therefore, claim 17 is rejected.

30. Regarding claim 18, Olarig discloses a set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor for delivering an interrupt request in a multi-node computer system, comprising: receiving an interrupt request at a scalability port switch(Figure 4, Component 312; Column 8, Lines 8-12; Since more components of type 312 can be used, it is scalable); determining an address of a scaleable node controller(Figure 4, Component 107, 306; More components of type 107 and 306 can be used and therefore it is scaleable) to receive said interrupt request; and transmitting said interrupt request to said scaleable node controller(Column 8, Lines 35-40; Column 9, Lines 57-65; LOPICs are bus agents that inherently have an address. By delivering the interrupt request to the destination LOPIC, an address has to be determined to deliver the interrupt request to the proper LOPIC). Olarig shows all of the elements recited in claim 18 and therefore, claim 18 is rejected.

31. Regarding claim 19, Olarig discloses a method of determining a processor to receive an interrupt request(Column 9, Lines 57-65), Olarig shows all of the elements recited in claim 19 and therefore, claim 19 is rejected.

32. Regarding claim 20, Olarig discloses a method of comparing a priority of the processor's task with that of the interrupt request(Column 10, Lines 8-10). Olarig shows all of the elements recited in claim 20 and therefore, claim 20 is rejected.

33. Regarding claim 21, Olarig discloses a method for interrupting the processor(Column 10, Lines 10-13). Olarig shows all of the elements recited in claim 21 and therefore, claim 21 is rejected.

34. Regarding claim 23, Olarig discloses an interrupt request that is a broadcast interrupt(Column 9, Lines 56-67, and Column 10, Lines 1-7; A distributed delivery mode interrupt is a broadcast interrupt). Olarig shows all of the elements recited in claim 23 and therefore, claim 23 is rejected.

35. Regarding claim 24, Olarig discloses the use of an end of interrupt register to indicate the end of processing of an interrupt(Column 7, Lines 50-55). Olarig shows all of the elements recited in claim 24 and therefore, claim 24 is rejected.

36. Regarding claim 25, Olarig discloses an interrupt request that is generated by a PCI device. generates an interrupt request(Column 8, Line 17; Since Olarig discloses a PCI bus(Figure 4, 113; Column 8, Line 1), it is inherent Olarig's system comprises a PCI device that will generate an interrupt). Olarig shows all of the elements recited in claim 25 and therefore, claim 25 is rejected.

37. Regarding claim 26, Olarig discloses a method, wherein the interrupt request is generated by a processor(Column 7, Lines 28-30). Olarig shows all of the elements recited in claim 26 and therefore, claim 26 is rejected.

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

40. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavallaei, in view of Neal et al.(US Patent 6,119,191), hereinafter referred to as Neal.

41. Regarding claim 4, Tavallaei discloses of an input/output hub(Figure 1, Component 28; Devices are connected to component 28 and therefore can act as an input/output hub) coupled between the PCI bus and the port switch. Tavallaei does not disclose multiple PCI hubs connected to the input/output hub. However, Neal discloses multiple PCI hubs that are connected

to a hub(Figure 5). Therefore, it would have been obvious to combine the teachings of Tavallaei with the teachings of Neal because this would allow more PCI devices to be connected.

42. Regarding claim 5, Tavallaei discloses a second pair of node controllers coupled to a switch(Figure 1, Component 14).

43. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavallaei and Neal as applied to claims 4-5 above, and further in view of Multiprocessor Specification, hereinafter referred to as MP.

44. Regarding claims 6 and 7, Tavallaei and Neal do not disclose the use of an additional switch connected to the first input/output hub. However, MP discloses the use of multiple switches(Figure 2-2; I/O APIC). Therefore it would be obvious to combine the teachings of Tavallaei and Neal with the teachings of Olarig to have a second port switch connected to the first input/output hub because it would interrupt scalability(Page 3-13).

45. Claims 13 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavallaei, in view of Arndt et al.(US Patent 6,189,065), hereinafter referred to as Arndt.

46. Regarding claim 13, Tavallaei does not disclose the method of redirecting the interrupt request to a different processor. However, Arndt discloses redirecting an interrupt to a different processor(Column 8, Claim 8). Therefore it would have been obvious to combine the teachings of Arndt and Tavallaei to redirect an interrupt to different processor since this would allow an interrupt to be handled faster than waiting for the original, busy processor to handle the interrupt.

47. Regarding claim 22, Tavallaei does not disclose the method of redirecting the interrupt request to a different processor. However, Arndt discloses redirecting an interrupt to a different processor(Column 8, Claim 8). Therefore it would have been obvious to combine the teachings

of Arndt and Tavallaei to redirect an interrupt to different processor since this would allow an interrupt to be handled faster than waiting for the original, busy processor to handle the interrupt.

48. Claims 13 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig, in view of Arndt.

49. Regarding claim 13, Olarig does not disclose the method of redirecting the interrupt request to a different processor. However, Arndt discloses redirecting an interrupt to a different processor(Column 8, Claim 8). Therefore it would have been obvious to combine the teachings of Arndt and Olarig to redirect an interrupt to different processor since this would allow an interrupt to be handled faster than waiting for the original, busy processor to handle the interrupt.

50. Regarding claim 22, Olarig does not disclose the method of redirecting the interrupt request to a different processor. However, Arndt discloses redirecting an interrupt to a different processor(Column 8, Claim 8). Therefore it would have been obvious to combine the teachings of Arndt and Olarig to redirect an interrupt to different processor since this would allow an interrupt to be handled faster than waiting for the original, busy processor to handle the interrupt.

Allowable Subject Matter

51. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

52. Applicant's arguments filed July 15, 2005 have been fully considered but they are not persuasive.

53. In response to applicant's argument that since the terminology used in the references is different from the claim language, the reference do not read on the claims. However, there is no clear definition of any of the components claimed. Therefore, examiner has broadly and reasonably interpreted the claim language.

54. In response to applicant's argument that Tavallaei's APIC 14 in figure 2 not being identical to a scaleable node controller and I/O APIC 26 of figure 4 not being identical to a scalability port switch, the fact that the terminology used for the components in the claim is different from the terminology used for the components in the reference is irrelevant since they both perform the same functions. Applicant has not clearly defined the terms "node controller" or "port switch" in the specification. I/O APIC distributes interrupts to the APICs and a APIC 14 controls interrupts for it's respective node and therefore I/O APIC and APIC 14 can be interpreted as a "port switch" and a "node controller," respectively. Further, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

55. In response to applicant's arguments of Tavallaei failing to teach a scalability port switch to determine an address of one of said scalable node controllers from said interrupt request,

Tavallaei discloses delivering interrupt data to an appropriate LOPIC, i.e. scalable node controller and determining the destination ID, i.e. address, of the LOPIC(Column 7, Lines 7-9, 54-56; Column 8, Lines 43-46). One of ordinary skill in the art would recognize that a destination ID is a term that can be used for address.

56. In response to applicant's arguments of Tavallaei failing to teach the limitation of comparing a priority of the interrupt request with a priority of the processor, Tavallaei discloses priorities associated with interrupts, which processor it is directed to(Column 7, Lines 41-44) and therefore the interrupt priority is compared with that of the processor and the task it is performing. It is inherent an interrupt request can only interrupt the processor if the interrupt request has a higher priority than the processor task being performed. This is further supported in the background section of the specification of the current application(Page 2, Lines 16-18).

57. In response to applicant's argument that Olarig's combined circuit of cache 107 and LOPIC 306 in figure 4 not being identical to a scaleable node controller and COPIC 314 of figure 4 not being identical to a scalability port switch, the fact that the terminology used for the components in the claim is different from the terminology used for the components in the reference is irrelevant since they both perform the same functions. Applicant has not clearly defined the terms "node controller" or "port switch" in the specification. I/O APIC distributes interrupts to the APICs and a APIC 14 controls interrupts for it's respective node and therefore I/O APIC and APIC 14 can be interpreted as a "port switch" and a "node controller," respectively. Further, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of

performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

58. In response to applicant's arguments of Olarig failing to teach a scalability port switch to determine an address of one of said scalable node controllers from said interrupt request, Olarig discloses delivering interrupt data to a LOPIC, i.e. scalable node controller and therefore would be determining the address of the LOPIC(Column 8, Lines 35-40; Column 9, Lines 57-65; LOPICs are bus agents that inherently have an address. By delivering the interrupt request to the destination LOPIC, an address has to be determined to deliver the interrupt request to the proper LOPIC).

59. In response to applicant's arguments of Olarig to teach the limitation of comparing a priority of the interrupt request with a priority of the processor, Olarig discloses the comparison of priorities of the processor and the interrupt(Column 3, Lines 4-7; Column 10, Lines 8-10). The specification of the current application discloses comparing priority of the processor as "compares the priority of the IRQ with the priority of the current processor task"(Page 8, Lines 11-12). Therefore Olarig discloses the method of comparing priority of the processor.

60. In response to applicant's arguments of Tavallaei failing to teach an input/output hub, the fact that the terminology used for the components in the claim is different from the terminology used for the components in the reference is irrelevant since they both perform the same functions. Applicant has not clearly defined the term "I/O Hub" in the specification. ASIC has inputs and outputs and therefore can be interpreted as a "I/O Hub." Further, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed

invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

61. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Arndt teaches redirecting an interrupt to another processor(Column 8, claim 8). Tavallaei discloses the I/O APIC, i.e. port switch distributing interrupts to the local APICs, i.e. node controllers. Therefore it would have been obvious the interrupt would have to be redirected through the I/O APIC, i.e. port switch.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP
May 12, 2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
5/12/06